II. Amendment to the Claims

Claims 1-23 are pending in the present application. No amendments are presented herein but the following listing and version of the claims is provided for ease of reference.

1. (previously presented) A metal-oxide-semiconductor device having a length and a width, comprising:

a semiconductor layer of a first conductivity type;

first and second source/drain regions of a second conductivity type formed in the semiconductor layer proximate an upper surface of the semiconductor layer and spaced laterally apart relative to one another along the length of said device, the first and second source/drain regions being formed in an active region of the device;

a gate formed above the semiconductor layer proximate the upper surface of the semiconductor layer and at least partially between the first and second source/drain regions, the gate being configured such that a dimension of the gate, defined substantially parallel to the width of the device, is confined to be substantially within the active region of the device; and

an isolation structure formed in the semiconductor layer, the isolation structure being configured to substantially isolate one or more portions of the first source/drain region from corresponding portions of the second source/drain region.

2. (original) The device of claim 1, wherein the isolation structure is configured to substantially prevent an inversion layer from being formed between the first and second source/drain regions when the device is turned off.

3. (original)The device of claim 1, wherein the isolation structure comprises a guard ring formed in the semiconductor layer proximate the upper surface of the semiconductor layer

between at least the one or more portions of the first and second source/drain regions, the guard ring being of the first conductivity type.

4. (original) The device of claim 3, wherein an impurity concentration of the guard ring is substantially matched to an impurity concentration of the semiconductor layer.

5. (original)The device of claim 4, wherein the impurity concentration of the guard ring is in a range from about 10^{18} to about 10^{19} atoms per cubic centimeter.

6. (original) The device of claim 1, wherein the isolation structure comprises at least one trench formed between at least the one or more portions of the first and second source/drain regions.

7. (original)The device of claim 1, wherein at least one of the one or more portions of the first and second source/drain regions comprises an end of the at least one of the first and second source/drain regions along a dimension substantially orthogonal to the gate.

8. (original)The device of claim 1, wherein the gate comprises a polysilicon layer and a salicide layer formed on at least a portion of the polysilicon layer.

9. (original)The device of claim 1, wherein the gate comprises a connection area for providing electrical connection to the gate, the connection area being proximate a middle portion of the gate along the dimension of the gate defined substantially parallel to at least one of the first and second source/drain regions.

10. (original)The device of claim 1, wherein the first source/drain region comprises a source of the device and the second source/drain region comprises a drain of the device.

11. (original)The device of claim 1, wherein the device comprises a diffused MOS (DMOS) device.

12. (original)The device of claim 1, wherein the device comprises a laterally diffused MOS (LDMOS) device.

13. (original)The device of claim 1, wherein the active region of the device is substantially defined within a thin insulating region of the device.

14. (previously presented)A method of forming a metal-oxide-semiconductor device having a length and a width, the method comprising the steps of:

forming first and second source/drain regions of a second conductivity type in a semiconductor layer of a first conductivity, the first and second source/drain regions being formed proximate an upper surface of the semiconductor layer and spaced laterally apart relative to one another along the length of said device, the first and second source/drain regions being formed in an active region of the device;

forming a gate above the semiconductor layer proximate the upper surface of the semiconductor layer and at least partially between the first and second source/drain regions, the gate being configured such that a dimension of the gate, defined substantially parallel to the width of said device, is confined to be substantially within the active region of the device; and

forming an isolation structure in the semiconductor layer, the isolation structure being configured to substantially isolate one or more portions of the first source/drain region from corresponding portions of the second source/drain region.

15. (original)The method of claim 14, wherein the step of forming the isolation structure comprises forming a guard ring in the semiconductor layer proximate the upper surface of the semiconductor layer between at least the one or more portions of the first and second source/drain regions, the guard ring being of the first conductivity type.

16. (original)The method of claim 15, wherein the step of forming the guard ring comprises matching an impurity concentration of the guard ring to an impurity concentration of the semiconductor layer.

17. (original)The method of claim 14, wherein the step of forming the isolation structure comprises configuring the isolation structure to substantially prevent an inversion layer from being formed between the first and second source/drain regions when the device is turned off.

18. (original)The method of claim 14, wherein the step of forming the isolation structure comprises forming at least one trench in the semiconductor layer between at least the one or more portions of the first and second source/drain regions.

19. (original)The method of claim 14, further comprising the step of forming a salicide layer on at least a portion of the gate, the salicide layer reducing a resistance of the gate.

20. (original)The method of claim 14, wherein the step of forming the gate comprises forming a connection area for providing electrical connection to the gate, the connection area being proximate a middle portion of the gate along the dimension of the gate defined substantially parallel to at least one of the first and second source/drain regions.

21. (previously presented)An integrated circuit including at least one metal-oxide-semiconductor (MOS) device having a length and a width, the at least one MOS device comprising:

a semiconductor layer of a first conductivity type;

first and second source/drain regions of a second conductivity type formed in the semiconductor layer proximate an upper surface of the semiconductor layer and spaced laterally

apart relative to one another along the length of said device, the first and second source/drain regions being formed in an active region of the device;

a gate formed above the semiconductor layer proximate the upper surface of the semiconductor layer and at least partially between the first and second source/drain regions, the gate being configured such that a dimension of the gate, defined substantially parallel to the width of said device, is confined to be substantially within the active region of the device; and

an isolation structure formed in the semiconductor layer, the isolation structure being configured to substantially isolate one or more portions of the first source/drain region from corresponding portions of the second source/drain region.

22. (original)The integrated circuit of claim 21, wherein the isolation structure is configured to substantially prevent an inversion layer from being formed between the first and second source/drain regions when the at least one MOS device is turned off.

23. (original)The integrated circuit of claim 21, wherein the isolation structure comprises a guard ring formed in the semiconductor layer proximate the upper surface of the semiconductor layer between at least the one or more portions of the first and second source/drain regions, the guard ring being of the first conductivity type.